IN THE CLAIMS:

Please AMEND claim 31 as shown below.

1. (Original) A communication device comprising:

an input port for receiving a data packet entering the communication device;

a look-ahead logic module configured to select an address of a first memory bank of an external memory device, wherein the look-ahead logic module is contained within an internal memory control device located within the communication device;

a pointer assignment module, connected to the look-ahead module, is configured to include an independent link list assigned exclusively to the first memory bank and to assign a pointer to the data packet based upon the first memory bank as determined by the look-ahead logic;

the internal memory control device configured to transfer the data packet to the external memory device; and

the pointer assignment module configured to return the pointer to the independent link list and update a free address pool when the pointer has been released after the data packet has been transferred from the external memory device.

2. (Original) The communication device as recited in claim 1, wherein the communication device comprises a switch.

3. (Original) The communication device as recited in claim 1, wherein the previous request operation is a write request.

4. (Original) The communication device as recited in claim 1, wherein the previous request operation is a read request.

5. (Original) The communication device as recited in claim 1, further comprising:

a medium access control (MAC) protocol module having a MAC address for transmitting the data packet, wherein the MAC connects to the internal memory device;

a layer two switching module configured to build a table of forwarding rules upon which the MAC addresses exist and to determine a packet size of the data packet, wherein the layer two switching module connects to the MAC; and

a memory buffer device, connected to the MAC, is configured to temporarily store the data packet if the packet size is smaller than a predetermined packet size.

6. (Original) The communication device as recited in claim 5, wherein the memory buffer device is further configured to aggregate the packet size of each successive data packet to generate data relating to a total packet size.

7. (Original) The communication device as recited in claim 6, wherein the memory buffer device is further configured to transfer each data packet stored therein to the internal memory control device when the total packet size exceeds the predetermined packet size.

8. (Original) A communication device comprising:

an input port for receiving the data packet entering the communication device;

a look-ahead logic module configured to override and assign a swapping address mapping scheme to select an address of a first memory bank of a memory device so that the data packet will not be assigned to a memory bank accessed in a previous request operation wherein the look-ahead logic module is contained within an internal memory control device located within the communication device;

a pointer assignment module, connected to the look-ahead module, is configured to assign a pointer to the data packet based upon the first memory bank determined by the look-ahead logic module; and

an output port, connected to the communication device, is configured to transfer the data packet to the memory bank of the memory device.

9. (Original) The communication device as recited in claim 8 wherein the communication device comprises a switch.

10. (Original) The communication device as recited in claim 8, wherein the previous request operation is a write request.

11. (Original) The communication device as recited in claim 8, wherein the previous request operation is a read request.

12. (Original) The communication device as recited in claim 8, further comprising:

a medium access control (MAC) protocol module having a MAC address for transmitting the data packet, wherein the MAC connects to the internal memory device;

a layer two switching module configured to build a table of forwarding rules upon which the MAC addresses exist and to determine a packet size of the data packet, wherein the layer two switching module connects to the MAC; and

a memory buffer device, connected to the MAC, configured to temporarily store the data packet if the packet size is smaller than a predetermined packet size.

13. (Original) The communication device as recited in claim 12, wherein the memory buffer device is further configured to aggregate the packet size of each successive data packet to generate data relating to a total packet size.

14. (Original) The communication device as recited in claim 13 wherein:

the memory buffer device is configured to transfer each data packet stored therein to a memory control device when the total packet size exceeds the predetermined packet size; and

the memory control device includes the look-ahead logic module.

15. (Original) A communication device comprising:

a look-ahead logic module configured to select an address of a first memory bank of a memory device so that no two successive request operations access the same memory bank wherein the look-ahead logic module is contained within an internal memory control device located within the communication device;

a pointer assignment module, connected to the look-ahead module, is configured to assign a pointer to the data packet based upon the first memory bank determined by the look-ahead logic module; and

an output port, connected to the communication device, is configured to transfer the data packet to the memory bank of the memory device.

16. (Original) The communication device as recited in claim 15, wherein the communication device comprises a switch.

17. (Original) The communication device as recited in claim 15, wherein the successive request operations are two successive write requests to access the same memory bank.

18. (Original) The communication device as recited in claim 15, wherein the successive request operations include a read request followed by a write request to access the same memory bank.

19. (Original) A communication device comprising:

a look-ahead logic module configured to select an address of a first memory bank of a memory device so that no two successive request operations access the same memory bank wherein the look-ahead module is contained within an internal memory control device located within the communication device;

a link list configured to include multiple independent link lists, wherein each link list is assigned exclusively to a predetermined memory bank located within the communication device;

a pointer assignment module, connected to the look-ahead module, is configured to assign a pointer from one of the independent link lists to the data packet based upon the first memory bank determined by the look-ahead logic module; and

an output port, connected to the communication device, is configured to transfer the data packet to the memory bank of the memory device.

20. (Original) The communication device as recited in claim 19, further comprising:

a medium access control (MAC) protocol module having a MAC address for transmitting the data packet, wherein the MAC connects to the internal memory device;

a layer two switching module configured to build a table of forwarding rules upon which the MAC address exist and to determine a packet size of the data packet, wherein the layer two switching module connects to the MAC; and

a cycle burst module configured to transfer the data packet to a memory buffer device if the packet size is smaller than a predetermined packet size to avoid a small packet write penalty, wherein the memory buffer device connects to the MAC.

21. (Original) The communication device as recited in claim 20, wherein the memory buffer device is further configured to aggregate the packet size of each successive data packet to generate data relating to a total packet size.

22. (Original) The communication device as recited in claim 21, wherein:

the memory buffer device is configured to transfer each data packet stored therein to a memory control device when the total packet size exceeds the predetermined packet size; and

the memory control device is configured to include the look-ahead logic module.

23. (Original) A method of assigning a data packet to a memory bank of an external memory device, the method comprising:

receiving the data packet at an input port of a communication device;

selecting an address of the memory bank of the external memory bank so that the data packet will not be assigned to a memory bank accessed in a previous request operation;

providing an independent link list assigned exclusively to the memory bank;

assigning a pointer to the data packet based upon the memory bank determined by the look-ahead logic;

transferring the data packet to the external memory device; and

returning the pointer to the independent link list and update a free address pool when the pointer has been released after the data packet has been transferred from the external memory device.

24. (Original) The method as recited in claim 23, wherein the communication device is a switch.

25. (Original) The method as recited in claim 23, wherein the previous request operation is a write request.

26. (Original) The method as recited in claim 23, wherein the previous request operation is a read request.

27. (Original) The method as recited in claim 23, further comprising:

storing the data packet temporarily in a memory buffer device if the packet size is smaller than a predetermined packet size.

28. (Original) The method as recited in claim 27, further comprising:

aggregating the packet size of each successive data packet to generate a total packet size.

29. (Original) The method as recited in claim 28, further comprising:

transferring each data packet stored within the memory buffer device to the internal memory control device when the total packet size exceeds the predetermined packet size.

30. (Original) A method of assigning a data packet to a memory bank of a memory device, the method comprising:

receiving the data packet at an input port of a communication device; overriding a swapping address mapping scheme to select and assign an address of the memory bank of

the memory device so that the data packet will not be assigned to a memory bank accessed in a previous request operation;

assigning a pointer to the data packet based upon the address of the memory bank determined; and

transferring the data packet to the memory bank of the memory device.

31. (Currently Amended) A method of assigning a data packet to a memory bank of a memory device, the method comprising:

receiving the data packet at an input port of a communication device;

selecting an address of the memory bank of the memory device so that no two successive request operations access the same memory bank[[.]];

assigning a pointer to the data packet based upon the memory bank determined by the look-ahead logic module; and

transferring the data packet to the memory bank of the memory device.

32. (Original) The method as recited in claim 31, wherein the communication device is a switch.

33. (Original) The method as recited in claim 31, wherein the successive request operations are two successive write requests to access the same memory bank.

34. (Original) The method as recited in claim 31, wherein the successive request operations include a read request followed by a write request to access the same memory bank.

35. (Original) A method of assigning a data packet to a memory bank of a memory device, the method comprising:

receiving the data packet at an input port of a communication device; selecting an address of the memory bank of the memory device so that no two successive request operations access the same memory bank;

providing a link list configured to include multiple independent link lists, wherein each link list is assigned exclusively to a predetermined memory bank;

assigning a pointer from one of the independent link lists to the data packet based upon the memory bank determined by the look-ahead logic module; and

transferring the data packet to the memory bank of the memory device.

36. (Original) The method as recited in claim 35, further comprising:

providing a cycle burst module configured to transfer the data packet to a memory buffer device if the packet size is smaller than a predetermined packet size to avoid a small packet write penalty.

37. (Original) A communication device comprising:

receiving means for receiving the data packet at an input port of a communication device, entering the communication device;

selecting means for selecting an address of a first memory bank of the external memory bank so that the data packet will not be assigned to a memory bank accessed in a previous request operation;

providing means for providing an independent link list assigned exclusively to the first memory bank;

assigning means for assigning a pointer to the data packet based upon the first memory bank determined by the look-ahead logic;

transferring means for transferring the data packet to an external memory device; and

returning means for returning the pointer to the independent link list and updating a free address pool when the pointer has been released after the data packet has been transferred from the external memory device.

38. (Original) The communication device as recited in claim 37, wherein the communication device comprises a switch.

39. (Original) The communication device as recited in claim 37, wherein the previous request operation is a write request.

40. (Original) The communication device as recited in claim 37, wherein the previous request operation is a read request.

41. (Original) The communication device as recited in claim 37, further comprising: storing means for storing the data packet temporarily in a memory buffer device if the packet size is smaller than a predetermined packet size.

42. (Original) The network as recited in claim 41, further comprising:

aggregating means for aggregating the packet size of each successive data packet to generate a total packet size.

43. (Original) The communication device as recited in claim 42, further comprising:

transferring means for transferring each data packet stored within the memory buffer device to the internal memory control device when the total packet size exceeds the predetermined packet size.

44. (Original) A communication device comprising:

receiving means for receiving the data packet at an input port of a communication device;

overriding means for overriding a swapping address mapping scheme to select and assign an address of the memory bank of a first memory device so that the data packet will not be assigned to the memory bank accessed in a previous request operation;

assigning means for assigning a pointer to the data packet based upon the address of the memory bank determined; and

transferring means for transferring the data packet to the memory bank of the first memory device.

45. (Original) A communication device comprising:

receiving means for receiving the data packet at an input port of a communication device;

selecting means for selecting an address of a first memory bank of a memory device so that no two successive request operations access the same memory bank;

assigning means for assigning a pointer to the data packet based upon the first memory bank determined by the look-ahead logic module; and

transferring means for transferring the data packet to the first memory bank of the memory device.

46. (Original) The communication device as recited in claim 45, wherein the communication device comprises a switch.

47. (Original) The communication device as recited in claim 45, wherein the successive request operations are two successive write requests to access the same memory bank.

48. (Original) The communication device as recited in claim 45, wherein the successive request operations include a read request followed by a write request to access the same memory bank.

49. (Original) A communication device comprising:

receiving means for receiving the data packet at an input port of a communication device;

selecting means for selecting an address of a first memory bank of a memory device so that no two successive request operations access the same memory bank;

providing means for providing a link list configured to include multipleindependent link lists, wherein each link list is assigned exclusively to a predetermined memory bank;

assigning means for assigning a pointer from one of the independent link lists to the data packet based upon the first memory bank determined by the look-ahead logic module; and

transferring means for transferring the data packet to the first memory bank of the memory device.

50. (Original) The communication device as recited in claim 49, further comprising:

providing means for providing a cycle burst module configured to transfer thedata packet to a memory buffer device if the packet size is smaller than a predetermined packet size to avoid a small packet write penalty.

51. (Original) A communication device comprising:

an input port for receiving the data packet entering the communication device;

a look-ahead logic module configured to select an address of a first memory bank of a memory device by overriding an address mapping scheme that permits successive data packets to be assigned to the same memory bank, wherein the look-ahead logic module is contained within an internal memory control device located within the communication device;

a pointer assignment module, connected to the look-ahead module, is configured to assign a pointer to the data packet based upon the memory bank determined by the look-ahead logic module; and

an output port, connected to the communication device, is configured to transfer the data packet to the memory bank of the memory device.

52. (Original) The communication device as recited in claim 51, wherein the mapping scheme is an address swapping mapping scheme.

53. (Original) A method of assigning a data packet to a memory bank of a memory device, the method comprising:

receiving the data packet at an input port of a communication device; selecting an address of the memory bank of the memory device by overriding an address mapping scheme that permits successive data packets to be assigned to the same memory bank;

assigning a pointer to the data packet based upon the memory bank determined by the look-ahead logic module; and

transferring the data packet to the memory bank of the memory device.

54. (Original) The method as recited in claim 53, wherein the mapping scheme is an address swapping mapping scheme.

55. (Original) A communication device comprising:

receiving means for receiving the data packet at an input port of a communication device;

selecting means for selecting an address of a first memory bank of a memory device by overriding an address mapping scheme that permits successive data packets to be assigned to the same memory bank;

assigning means for assigning a pointer to the data packet based upon the first memory bank determined by the look-ahead logic module; and

transferring means for transferring the data packet to the first memory bank of the memory device.

56. (Original) The communication device as recited in claim 55, wherein the mapping scheme is an address swapping mapping scheme.